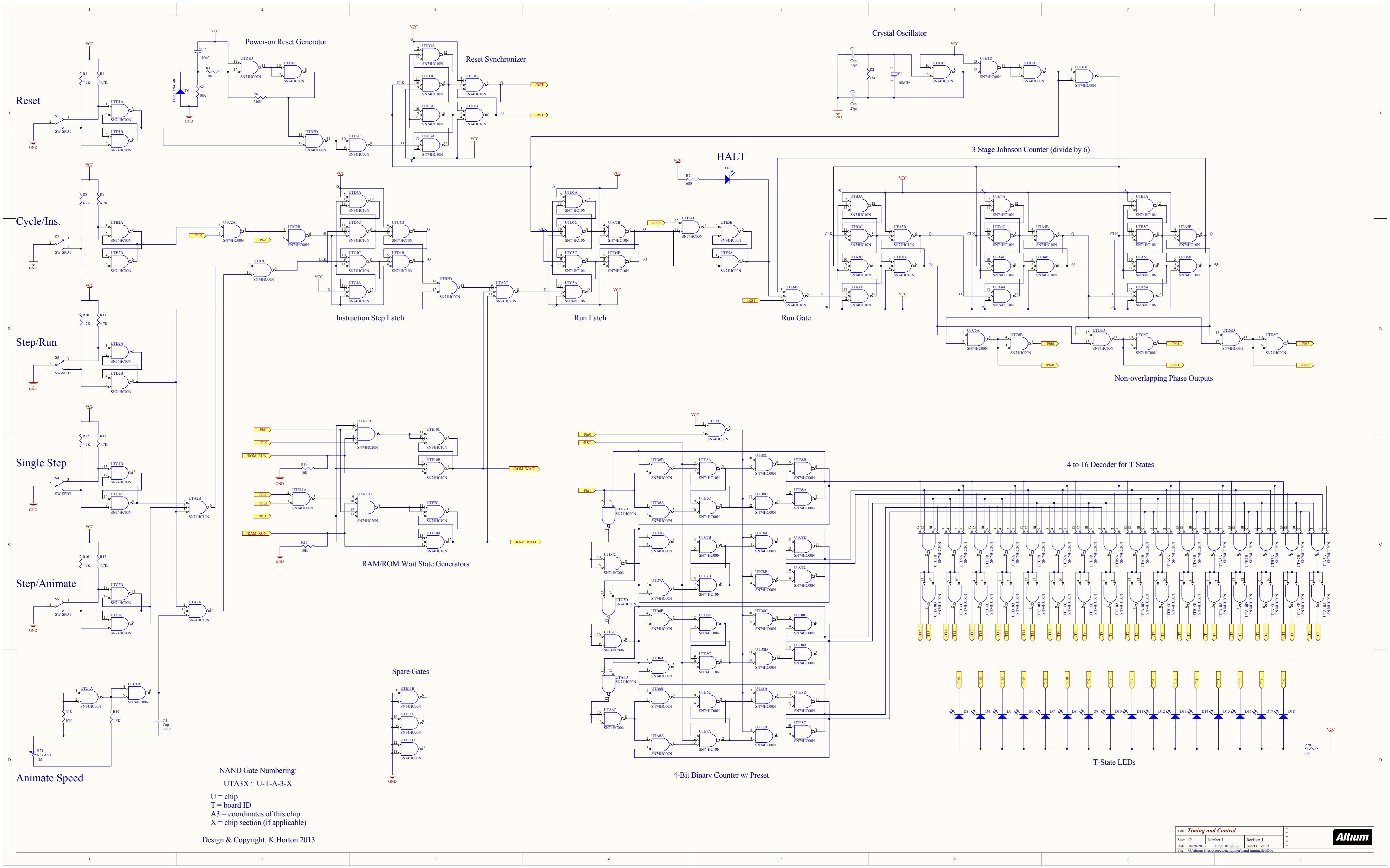
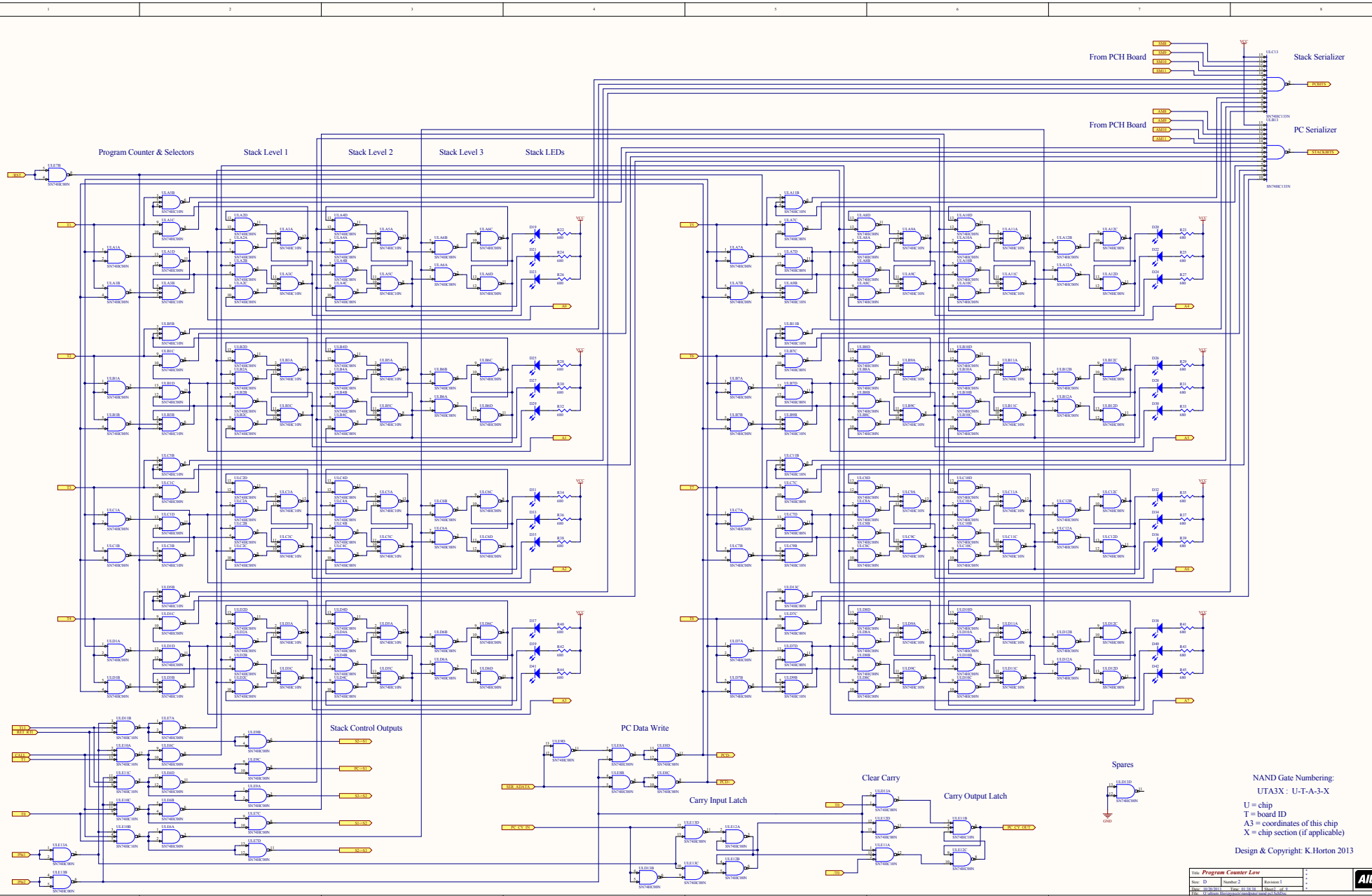
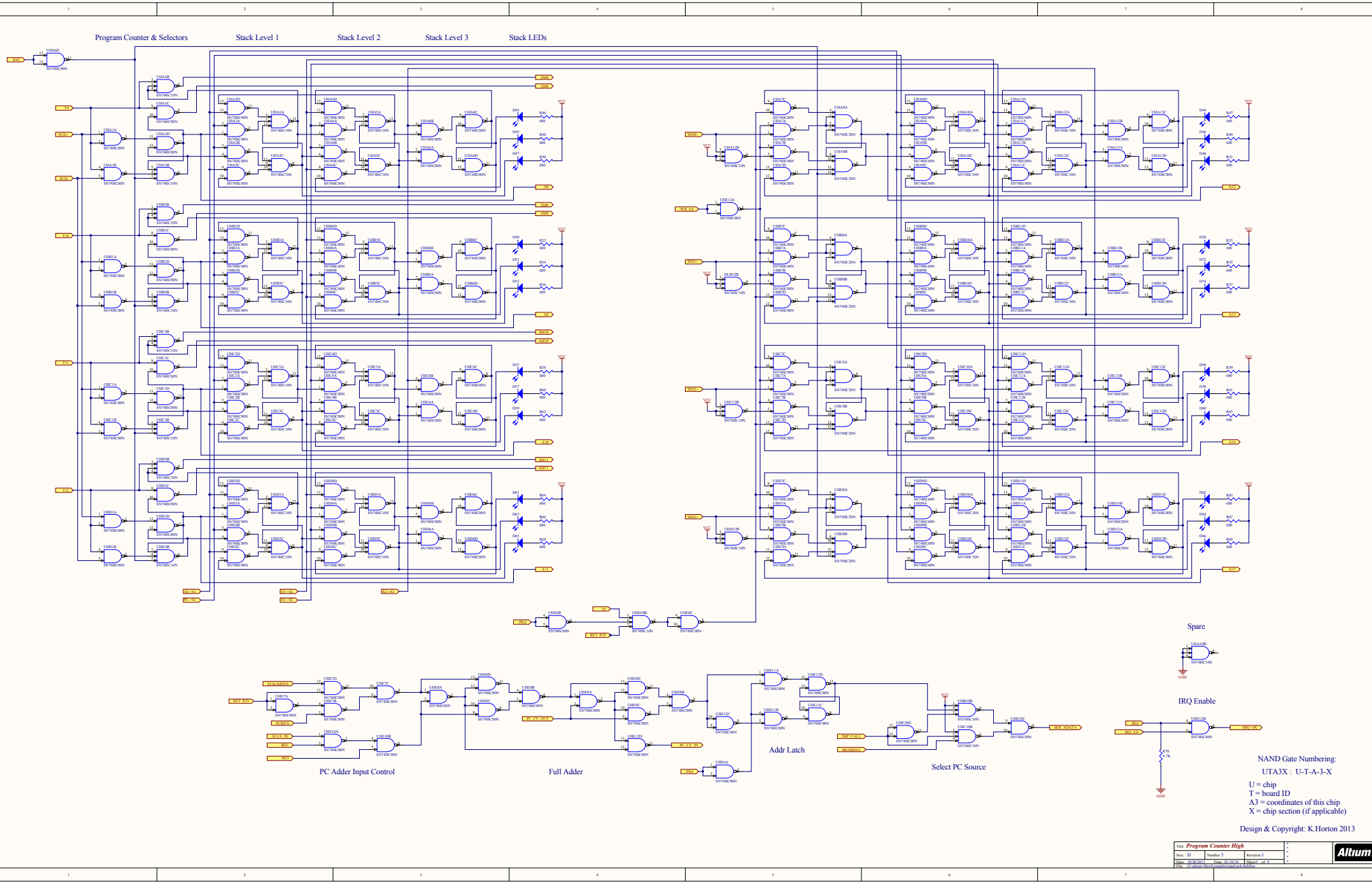
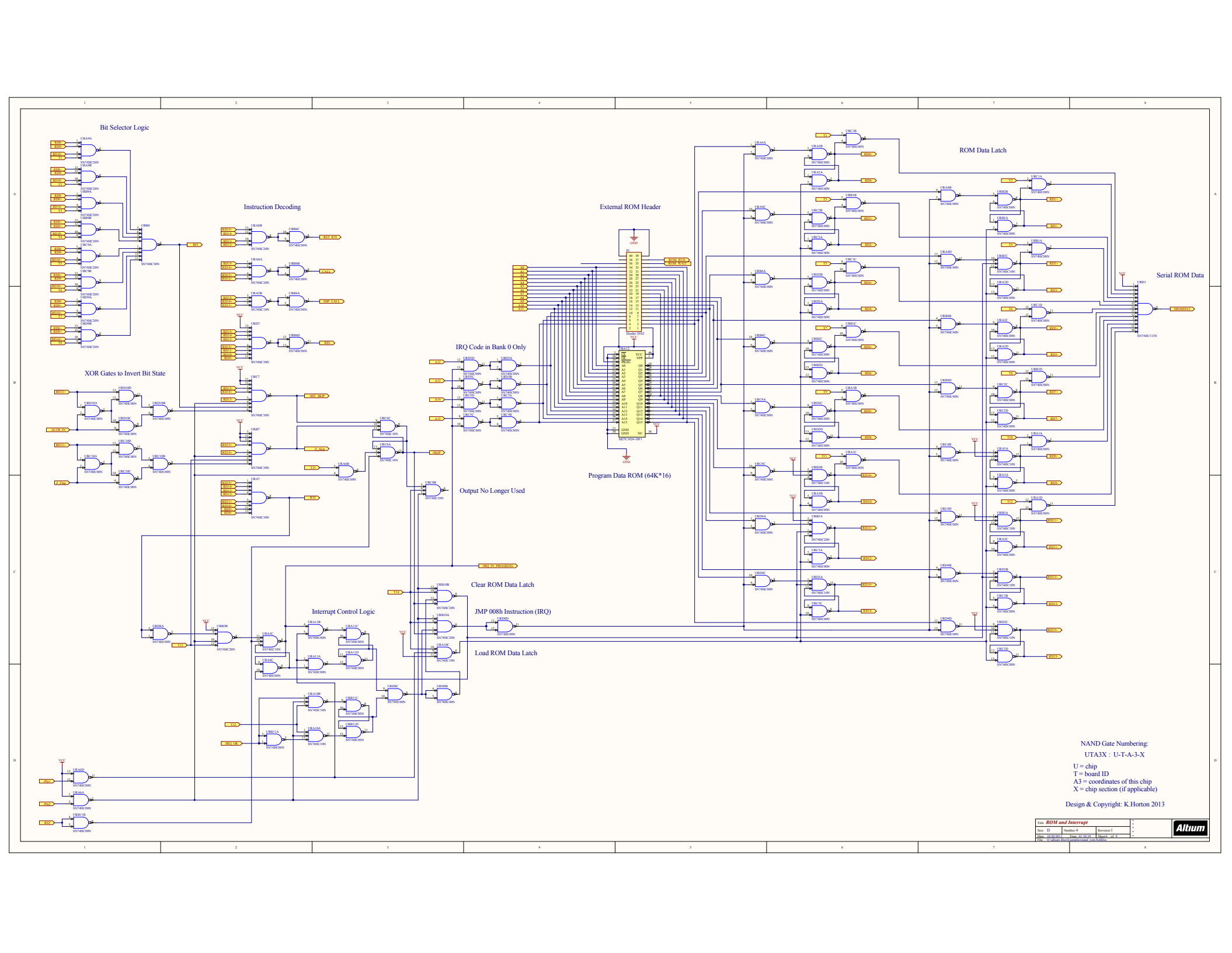
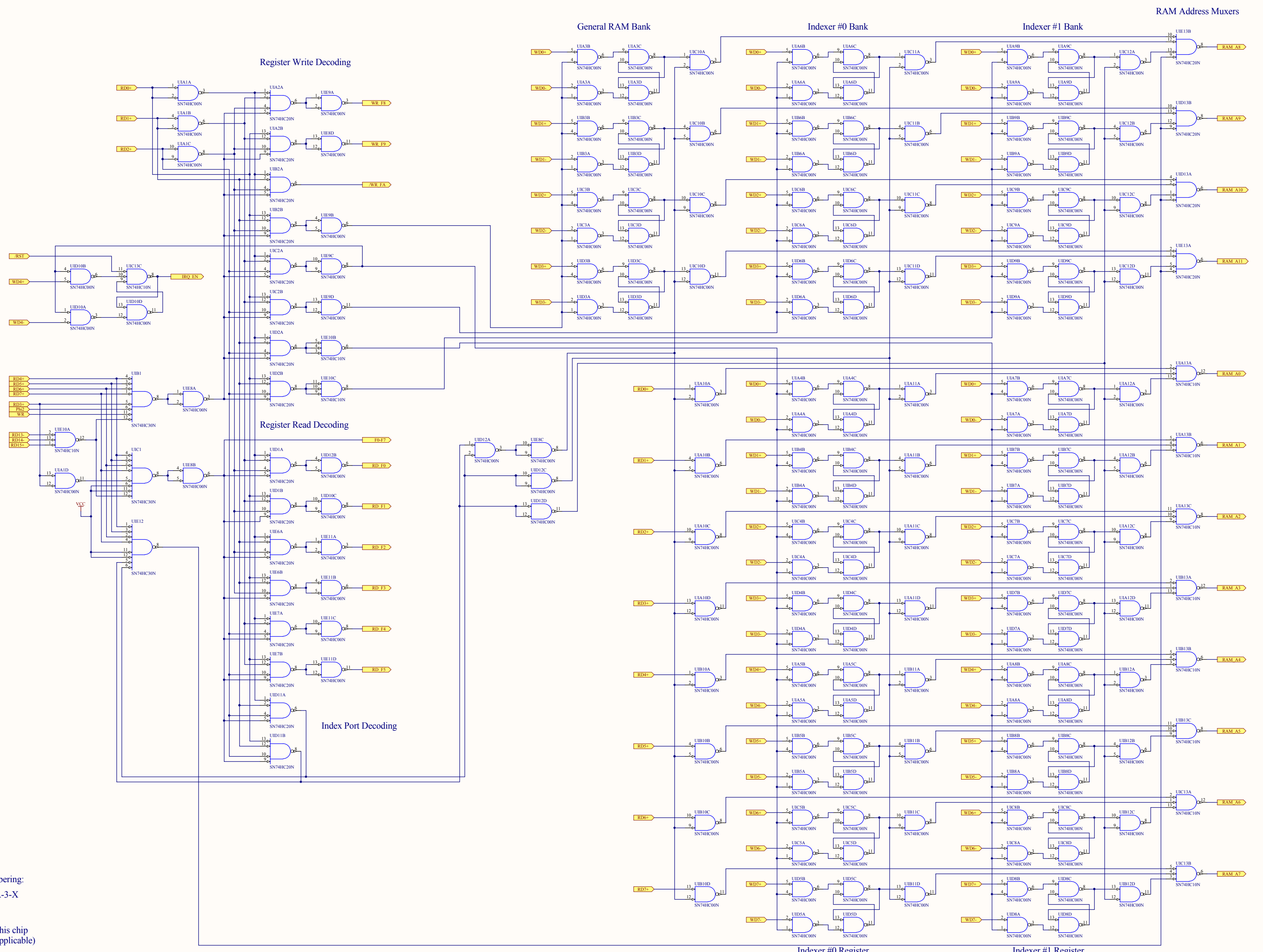

Reset
Cycle/Ins.
Step/Run
Single Step
Step/Animate
Animate Speed
Power-on Reset Generator
Reset Synchronizer
Crystal Oscillator
HALT
3 Stage Johnson Counter (divide by 6)
Instruction Step Latch
Run Latch
Run Gate
Non-overlapping Phase Outputs
RAM/ROM Wait State Generators
4 to 16 Decoder for T States
Spare Gates
4-Bit Binary Counter w/ Preset
T-State LEDs
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
Title Timing and Control
Altium


From PCH Board
Stack Serializer
From PCH Board
PC Serializer
Program Counter & Selectors
Stack Level 1
Stack Level 2
Stack Level 3
Stack LEDs
Stack Control Outputs
PC Data Write
Clear Carry
Carry Input Latch
Carry Output Latch
Spares
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
Program Counter Low
Altium


Program Counter & Selectors
Stack Level 1
Stack Level 2
Stack Level 3
Stack LEDs
Spare
IRQ Enable
PC Adder Input Control
Full Adder
Addr Latch
Select PC Source
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
Program Counter High
Altium


Bit Selector Logic
Instruction Decoding
External ROM Header
ROM Data Latch
Serial ROM Data
XOR Gates to Invert Bit State
IRQ Code in Bank 0 Only
Program Data ROM (64K*16)
Output No Longer Used
Interrupt Control Logic
Clear ROM Data Latch
JMP 008h Instruction (IRQ)
Load ROM Data Latch
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
ROM and Interrupt
Altium

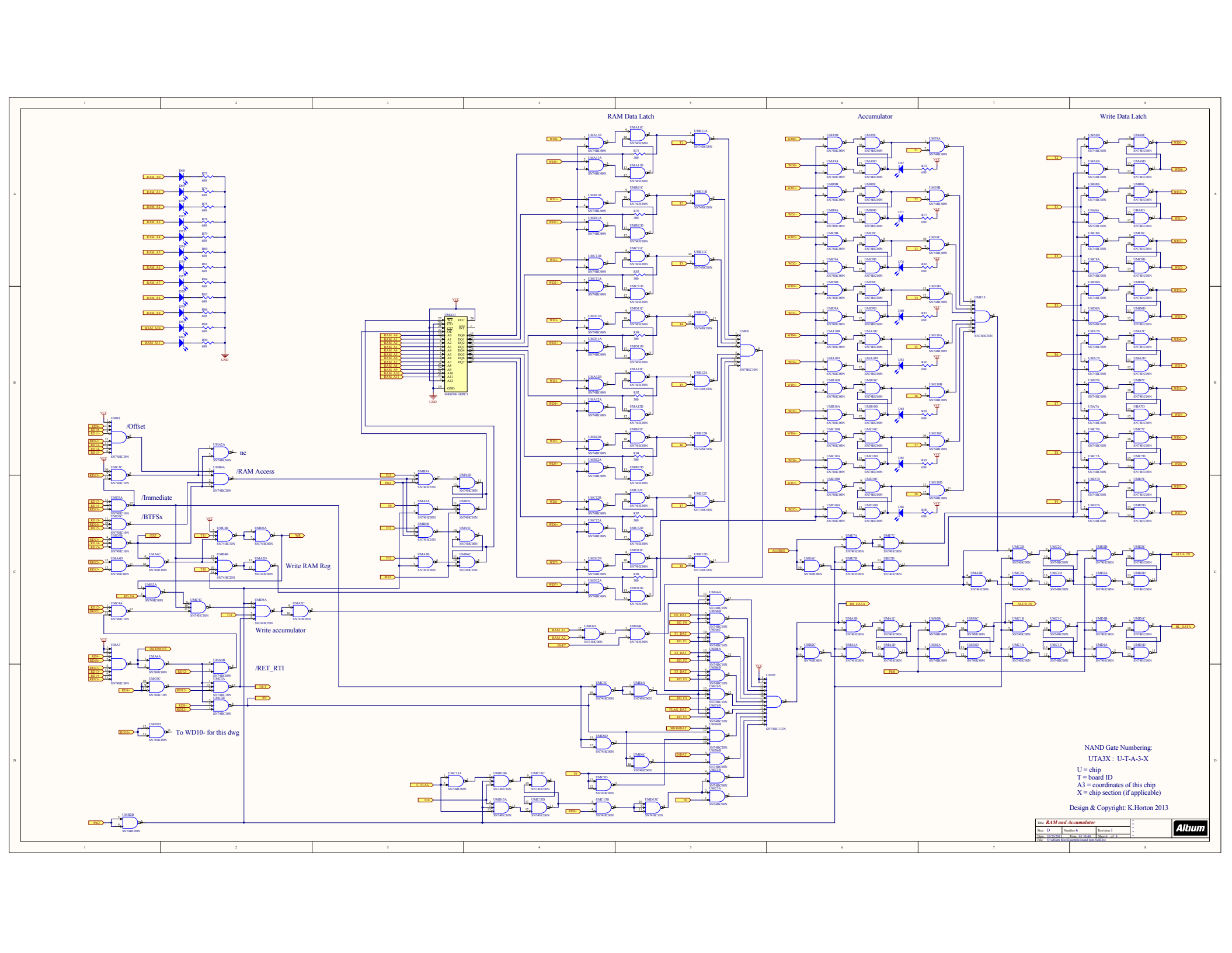


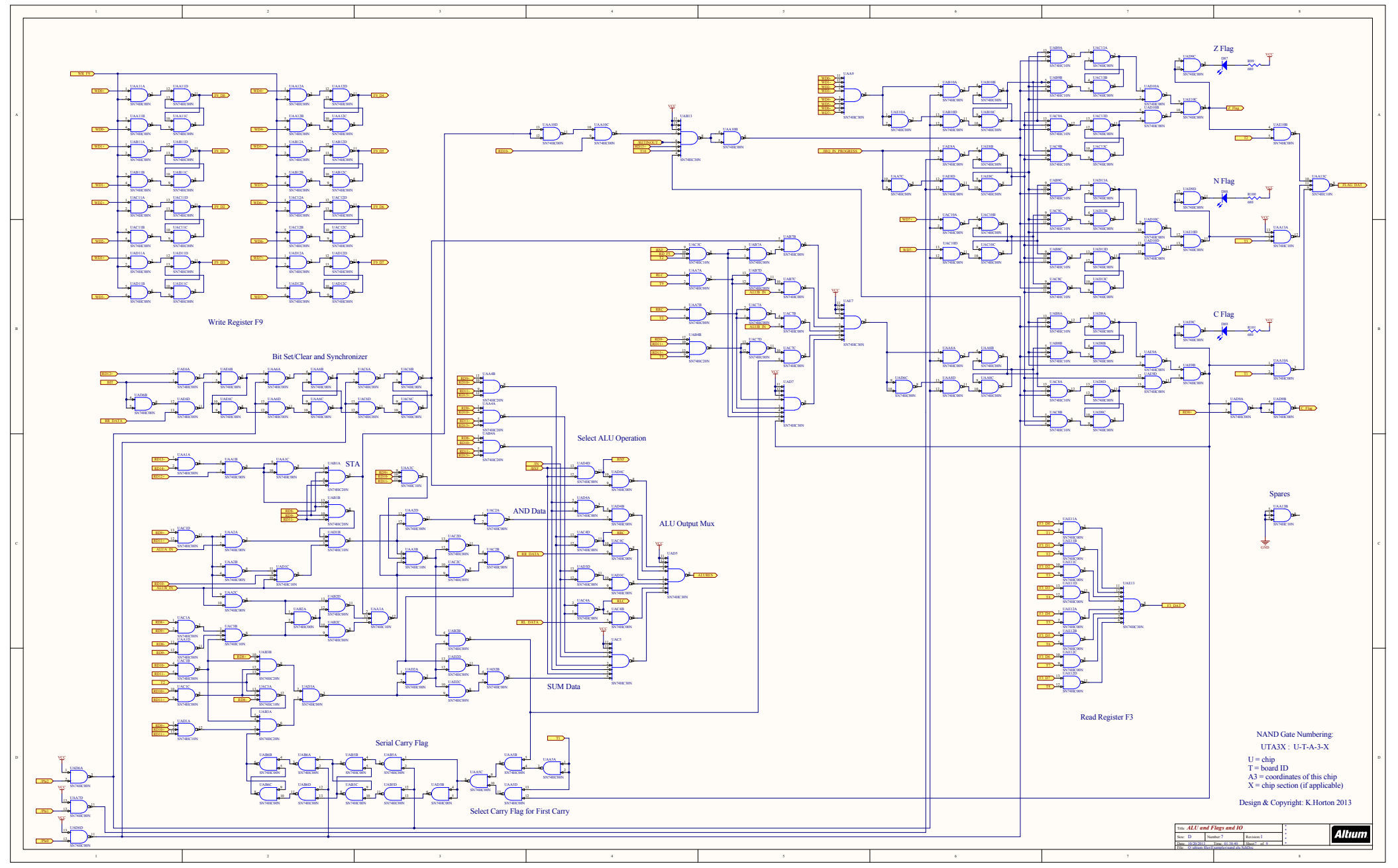
NAND Gate Numbering:

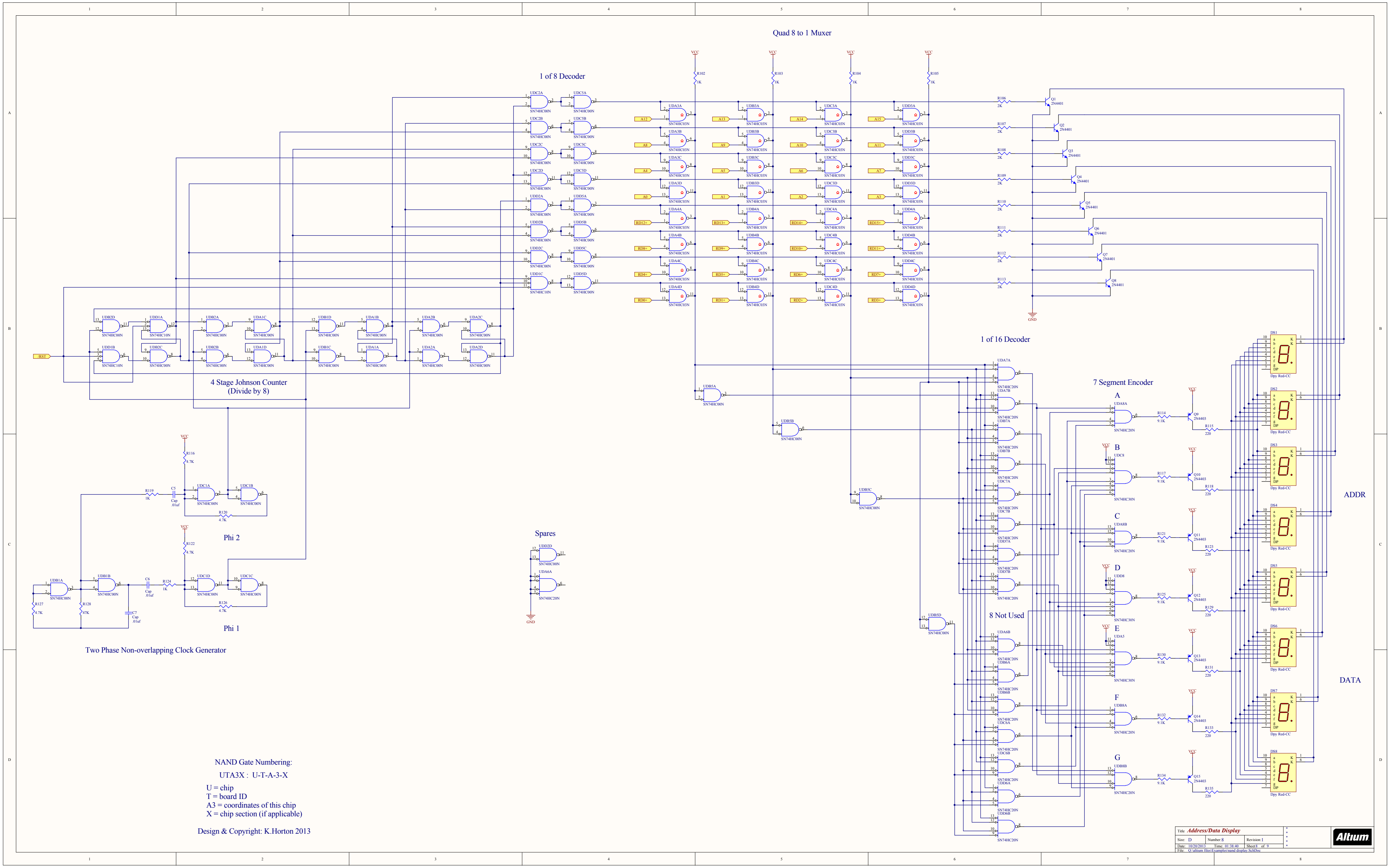
UTA3X : U-T-A-3-X

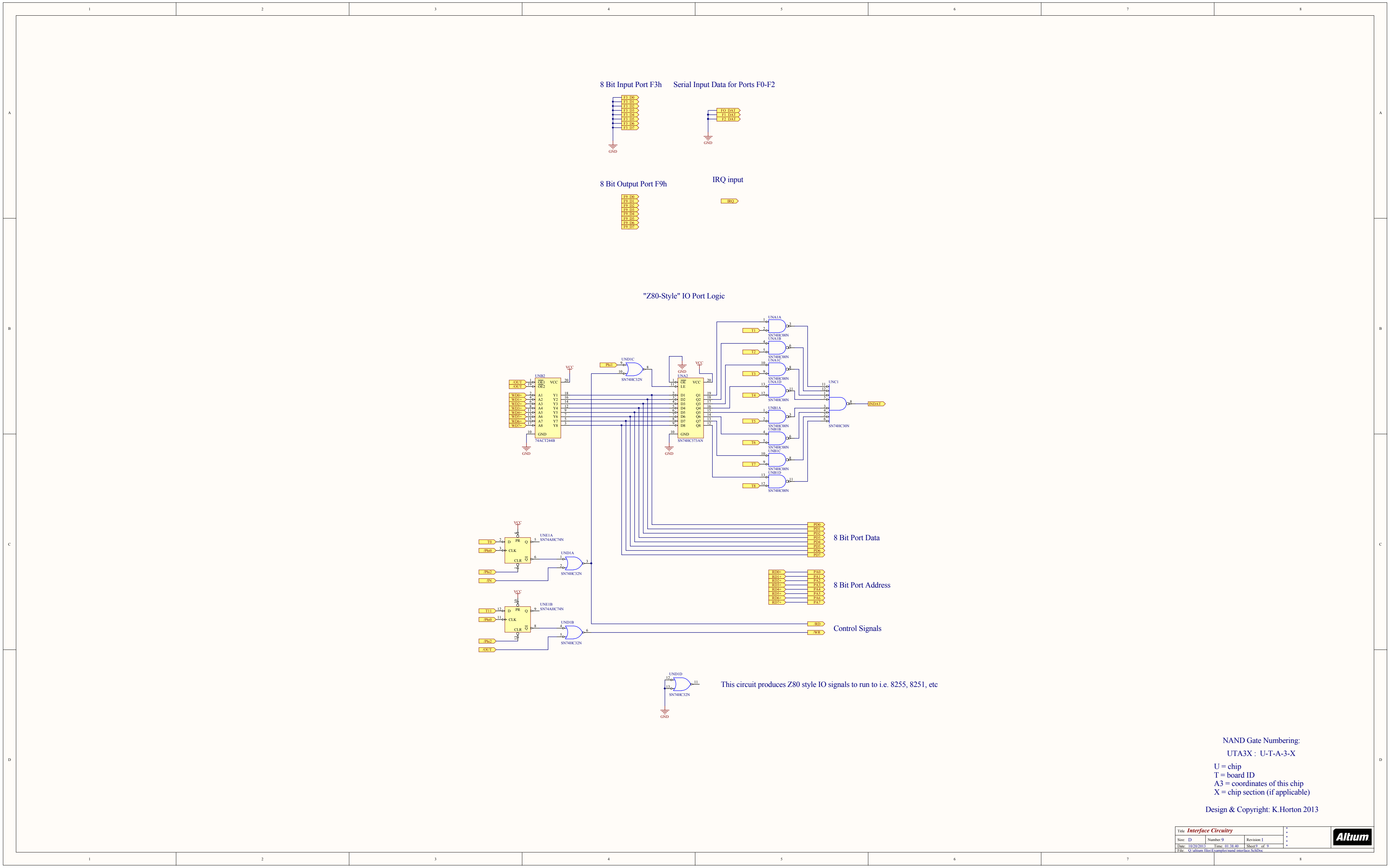
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)

Title: Indexer / Address Decode		
Size: D	Number: 5	Revision: 1
Date: 10/20/2013 Time: 01:38:39		Sheet 5 of 9
File: Q:\altium files\Examples\nand indexer.SchDoc		


RAM Data Latch
Accumulator
Write Data Latch
/Offset
nc
/RAM Access
/Immediate
/BTFSx
Write RAM Reg
Write accumulator
/RET_RTI
To WD10- for this dwg
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
RAM and Accumulator
Altium


Write Register F9
Bit Set/Clear and Synchronizer
STA
AND Data
Select ALU Operation
ALU Output Mux
SUM Data
Serial Carry Flag
Select Carry Flag for First Carry
Read Register F3
Z Flag
N Flag
C Flag
Spares
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
ALU and Flags and IO
Altium


Quad 8 to 1 Muxer
1 of 8 Decoder
1 of 16 Decoder
7 Segment Encoder
A
B
C
D
E
F
G
ADDR
DATA
8 Not Used
Spares
4 Stage Johnson Counter
(Divide by 8)
Phi 2
Phi 1
Two Phase Non-overlapping Clock Generator
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
Title Address/Data Display
Size: D
Number: 8
Revision: 1
Date: 10/20/2013
Time: 01:38:40
Sheet 8 of 9
File: Q:\altium files\Examples\nand display.SchDoc



8 Bit Input Port F3h
Serial Input Data for Ports F0-F2
8 Bit Output Port F9h
IRQ input
"Z80-Style" IO Port Logic
SN74HC00N
SN74HC32N
SN74HC573AN
74ACT244B
SN74AHC74N
8 Bit Port Data
8 Bit Port Address
Control Signals
This circuit produces Z80 style IO signals to run to i.e. 8255, 8251, etc
NAND Gate Numbering:
UTA3X : U-T-A-3-X
U = chip
T = board ID
A3 = coordinates of this chip
X = chip section (if applicable)
Design & Copyright: K.Horton 2013
Title Interface Circuitry
Size: D
Number: 9
Revision: 1
Date: 10/20/2013
Time: 01:38:40
Sheet 9 of 9
File: Q:\altium files\Examples\nand interface.SchDoc