

## RF/RP5H01

## CMOS 64 bit PROM

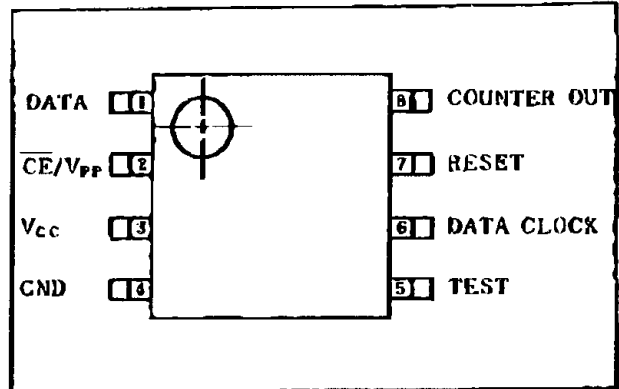
### ■ GENERAL DESCRIPTION

RP5H01/RP5H01 is a PROM with 64 × 1bit organization (+ dummy 8 bits), employing 2-layer silicon gate CMOS processing technology.

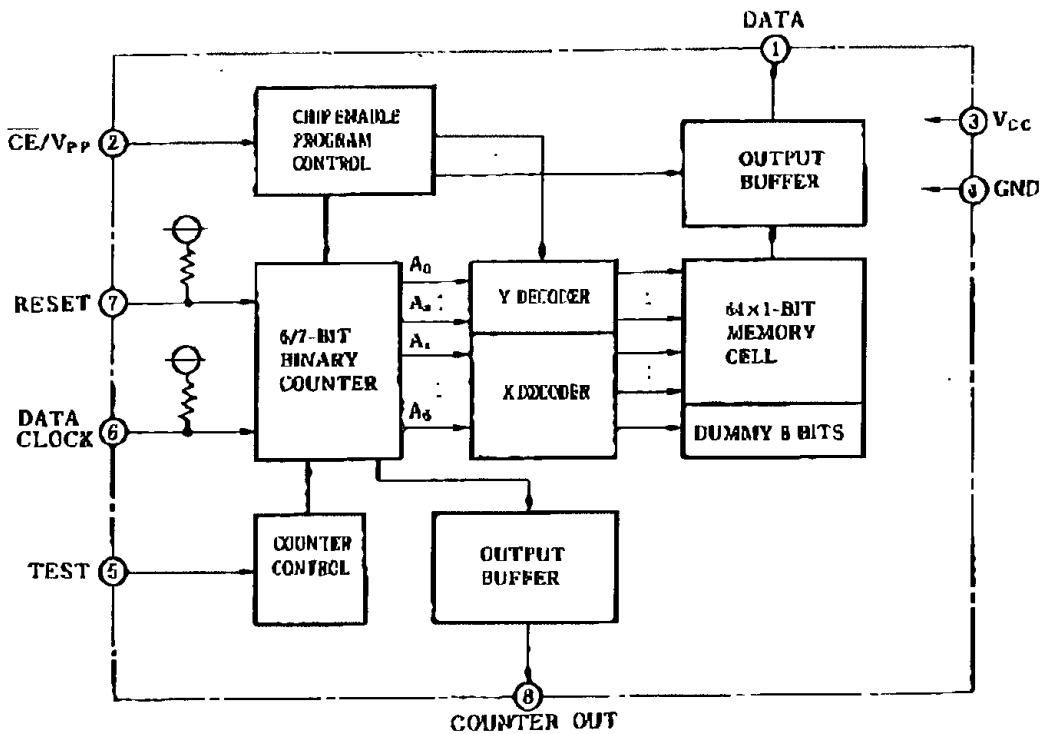
### ■ FEATURES

- 64 × 1bit organization (+ dummy 8 bits)
- Low power dissipation
  - Active 55mW (max)
  - Standby 550μW (max)
- Access time 1μs (max)
- Single power supply 5V ± 10%
- Serial outputs
- Inputs and outputs TTL level
- 3-state (Tri-state) outputs

### ■ PIN CONFIGURATION (Top view)



### ■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Limits	Unit
$V_{CC}$	$V_{CC}$ Supply Voltage	With respect to GND	-0.3~7	V
$V_{PP}$	$V_{PP}$ Supply Voltage		-0.3~22	V
$V_I$	Input Voltage		-0.3~7	V
$V_O$	Output Voltage		-0.3~7	V
$P_A$	Maximum Power Dissipation	$T_a = 25^\circ\text{C}$	0.3	W
$T_{OPR}$	Operating Temperature Range		-20~70	$^\circ\text{C}$
$T_{STG}$	Storage Temperature		-40~125	$^\circ\text{C}$

■ RECOMMENDED OPERATING CONDITIONS ( $T_a = -20 \sim 70^\circ\text{C}$ )

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V
$V_{OH}$	Input High Voltage	2.0		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	-0.1		0.8	V

■ ELECTRICAL CHARACTERISTICS

● READ OPERATION D.C. CHARACTERISTICS ( $T_a = -20 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ )

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC1}$	Standby $V_{CC}$ Supply Current		$CE/V_{PP} = V_{CC} \pm 0.3\text{V}$ DATA CLOCK, RESET = $V_{IL}$ or Open TEST = GND or $V_{CC} \pm 0.8\text{V}$			100	$\mu\text{A}$
$I_{CC2}$	Operating $V_{CC}$ Supply Current		$I_{OUT} = 0\text{mA}$			10	mA
$V_{OH}$	Output High Voltage		$I_{OH} = -400\mu\text{A}$	2.4			V
$V_{OL}$	Output Low Voltage		$I_{OL} = 2.1\text{mA}$			0.45	V
$V_{IH}$	Input High Voltage	Except TEST		2.0		$V_{CC} + 0.3$	V
		TEST		4.0		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	Except TEST		-0.1		0.8	V
		TEST		-0.1		1.0	V
$I_{LI}$	Input Leakage Current	RESET, DATA CLOCK	$V_I = 0\text{V}, V_{CC} = 5.5\text{V}$	-180		-20	$\mu\text{A}$
		TEST, $CE/V_{PP}$	$V_I = 0\text{V} \sim V_{CC}$	-10		10	$\mu\text{A}$
$I_{LO}$	Output Leakage Current		$V_O = 0\text{V} \sim V_{CC}$	-10		10	$\mu\text{A}$

● READ OPERATION, A.C. CHARACTERISTICS ( $T_a = -20 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ )

Symbol	Parameters	Test Conditions	Limits			Unit
			Min	Typ	Max	
$t_{AOC}$	Clock to Output Delay	$CE/V_{PP} = V_{IL}$			1	$\mu\text{s}$
$t_{CE}$	CE to Output Delay	Load = 1TTL + 10pF			1	$\mu\text{s}$
$t_{DF}$	CE High to Output Float		0		200	ns
$t_{RW}$	Reset pulse width		2			$\mu\text{s}$
$t_{CW}$	Clock pulse width		2			$\mu\text{s}$

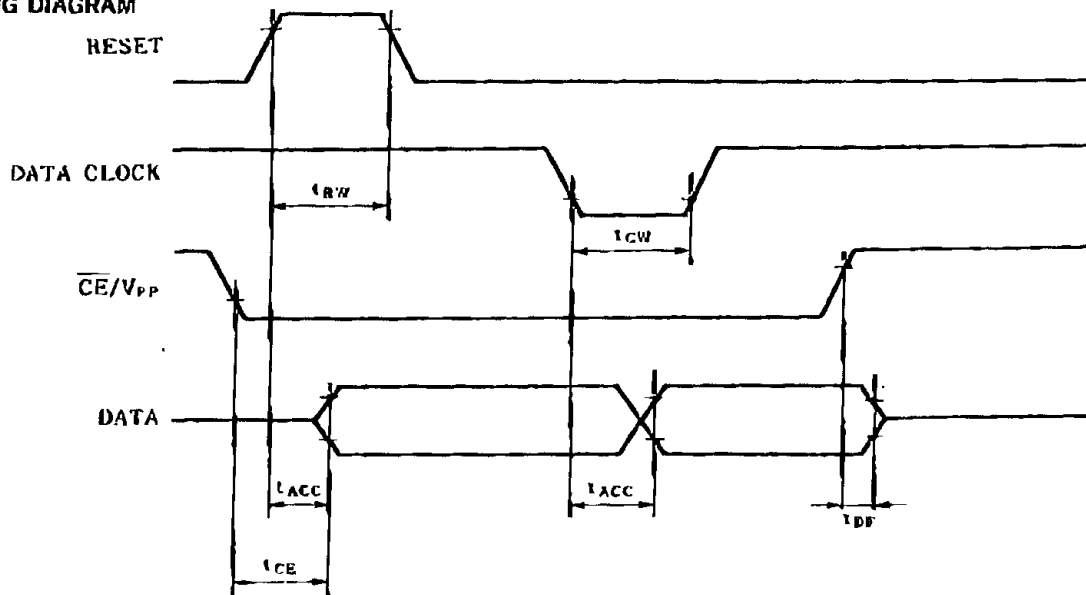
● D.C. PROGRAMMING CHARACTERISTICS ( $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$ )

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
$I_{PP}$	$V_{PP}$ Supply Current		$\overline{CE}/V_{PP} = V_{IHP}$			5	mA
$I_{CC}$	$V_{CC}$ Supply Current					0.5	mA
$V_{IH}$	Input High Voltage	Except TEST		2.0		$V_{IC} + 0.3$	V
		TEST		4.0		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	Except TEST		-0.1		0.8	V
		TEST		-0.1		1.0	V
$V_{IHP}$	Program pulse Input High Voltage			20.5	21.0	21.5	V
$V_{ILP}$	Program pulse Input Low Voltage			2.0	$V_{CC}$	6.0	V
$I_{II}$	Input leakage Current	RESET, DATA CLOCK	$V_I = 0\text{V}$ , $V_{CC} = 5.25\text{V}$	-170		-20	$\mu\text{A}$
		TEST	$V_I = 0\text{V} \sim V_{CC}$	-10		10	$\mu\text{A}$

● PROGRAMMING CHARACTERISTICS ( $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$ )

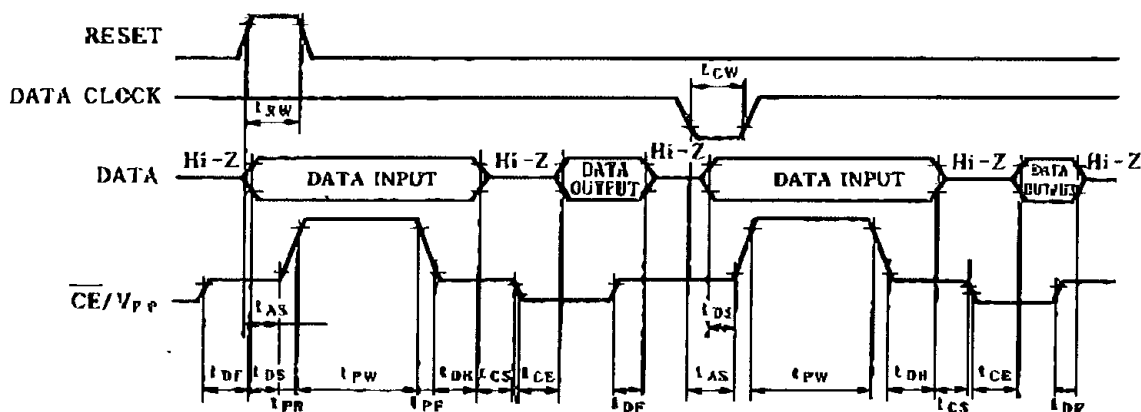
Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
$t_{AS}$	Address Set-up Time	2			$\mu\text{s}$
$t_{CS}$	CE Set-up Time	2			$\mu\text{s}$
$t_{DS}$	Data Set-up Time	2			$\mu\text{s}$
$t_{DH}$	Data Hold Time	2			$\mu\text{s}$
$t_{OF}$	CE to Output Float	0		200	ns
$t_{CD}$	CE to Output Delay			1	$\mu\text{s}$
$t_{PW}$	Program pulse width	45	50	55	ms
$t_{rA}$	$V_{PP}$ Pulse rise time	0.5		100	$\mu\text{s}$
$t_{fA}$	$V_{PP}$ Pulse fall time	0.5		100	$\mu\text{s}$
$t_{RW}$	Reset pulse width	2			$\mu\text{s}$
$t_{CW}$	Clock pulse width	2			$\mu\text{s}$

■ TIMING DIAGRAM



# RF/RP5H01

## ● PROGRAM MODE



## ■ OPERATING MODES

Mode	Pins	Data 1	Counter output 8	CE/V <sub>pp</sub> 2	V <sub>cc</sub> 3	GND 4
Read		Data Output	Clock (A5) Output	V <sub>IL</sub>	V <sub>CC</sub>	GND
Standby		High impedance	High impedance	V <sub>OH</sub>	V <sub>CC</sub>	GND
Program		Data Input	High impedance	V <sub>IRP</sub>	V <sub>CC</sub>	GND

	Counter operation mode
TEST (5) = GND	6 bits
TEST (5) = V <sub>CC</sub>	7 bits

## ■ EXPLANATION ON OPERATION

### ● READ MODE

RF5H01/RP5H01 is a serial address type PROM with 6-bit/7-bit counter. The first bit can be read out by adding reset pulse after CE/V<sub>pp</sub> = V<sub>IL</sub>. The 2nd bit—the 6th bit can be sequentially read out by adding data clock pulse. The output data is valid after a delay of t<sub>ACC</sub> from reset rise up or data clock fall down, in the state of CE/V<sub>pp</sub> = V<sub>IL</sub>.

In the state of TEST = GND, the counter operates as a 6-bit counter. It returns to the reset condition (address 000000), if it is added with 64-time data clock pulses after the reset pulse is applied.

The counter output pin is for operation test of the built-in counter. It puts out the highest output (A5) of the 6-bit counter.

### ● STANDBY MODE

RF5H01/RP5H01 is provided with power down function that is controlled by CE input. If TTL high level is given to the chip enable input (CE), the device comes to be the Standby Mode, and the output is in the state of high impedance.

### ● PROGRAM MODE

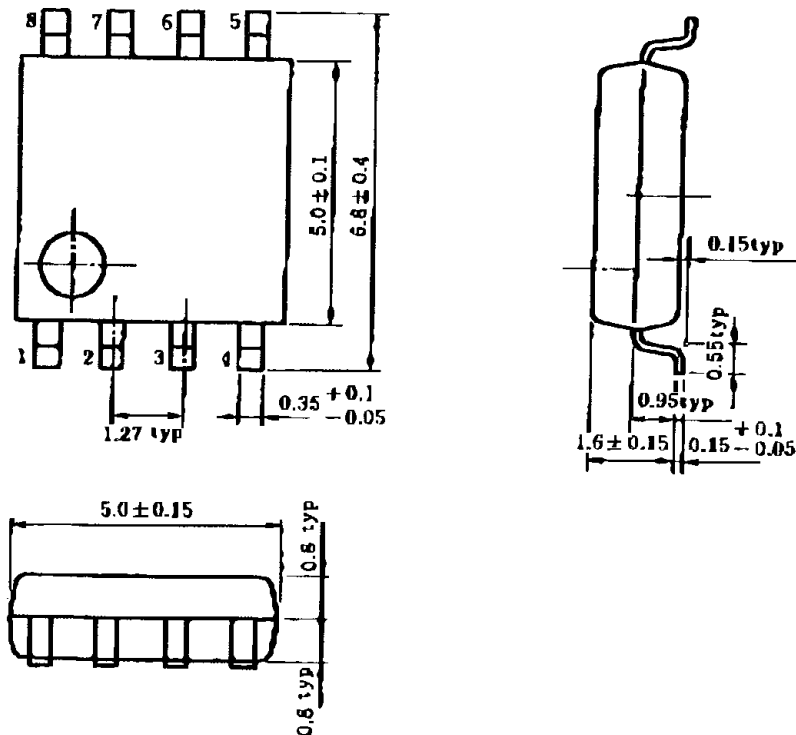
Initially, all bits of RF5H01/RP5H01 are in the "1" state. Data is introduced by selectively programming "0" into the desired bit locations.

The program is operated by setting up  $\overline{CE}/V_{PP} = V_{IH}$ , and adding the reset pulse, and then applying the 50mS 21V program pulse. The data are verified by making  $\overline{CE}/V_{PP} = V_{IL}$ . The 2nd bit ~ the 64th bit are programmed by progressing the addresses in sequence by means of adding the data clock pulse.

### ● DUMMY BITS

RF5H01/RP5H01 is a one-time PROM. For this reason, it is provided with a dummy bit of 8 bits for test programming. The dummy bit is located after the practical use 64th bit. The address is 8 bits of 1000000~1000111. The built-in counter operates as a 7-bit counter when "Test" (5 pins) is set at  $V_{CC}$  level, enabling to select the dummy bit. In the case of the "Test" being GND level, the counter operates as the 6-bit counter, being unable to select the dummy bit. In the 7-bit counter, when the clock pulse is added in sequence, the address progresses from 0000000 to 1111111, and then returns to 0000000.

### ■ 8-PIN PLASTIC FLAT PACKAGE (EXTERNAL VIEW) (UNIT : mm)



■ 8-PIN PLASTIC DIL PACKAGE (EXTERNAL VIEW) (UNIT : mm)

